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A Common-Source Input Stage-Based Transimpedance Amplifier for Fiber Optical Systems

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ABSTRACT

A simulated transimpedance amplifier (TIA) is proposed in this work with analytical derivations. The common source (CS) input stage proved to show extremely low power consumption and input-referred noise current (spectral density) with high TIA gain and moderate f_(-3dB) bandwidth. A value of 56.8 dBΩ in TIA gain magnitude is reported at a bandwidth (BW) of 1 GHz. A low 0.41 mW of total power consumption was achieved, corresponding to the 15.3 pA⁄√(H_z) well reduced magnitude. A specific trade-off relaxation property appears to have occurred between TIA gain and input referred noise current on one hand, while on the other hand, a combinational low power consumption and input referred noise current took place. The above key findings represent the valuable solutions for the main challenges in industrial applications, especially in reducing TIA power consumption, as application-specific, demand with high integrity signals involving low input referred noise current.

Keywords: TIA circuit, front-end topology, CS structure, optical pre-amplifier, transimpedance.

INTRODUCTION

For decades, transimpedance amplifiers (TIAs) have been widely used as the key front-end circuits for optical communications and sensors, which with no exception, involve many design trade-offs among the gain, bandwidth, noise, supply voltage, and power consumption. Traditionally, the priority due to the limited f_T of CMOS technology is obtaining sufficient bandwidth with small gain ripples and acceptable input-referred noise (Gu *et al.*, 2023). The common source (CS) amplifier and a shunt-feedback circuit are often the fundamental components of the basic TIA (Mohan *et al.*, 2000; Anusha *et al.*, 2018). The importance of Transimpedance amplifiers (TIAs) is that the small currents generated by the photodiode can be transformed into a voltage through it. It's principally useful when dealing with high-impedance current sources, such as sensors or photodiodes. Dealing with TIAs is due to two main reasons: The first is the sources of high impedance, as some sensors generate a current signal with a high output impedance, and the second reason is the accurate measurement of the current, because TIAs provide a low input impedance, which ensures accurate measurement of the current signal. The challenge is to maintain a wide bandwidth while ensuring minimal noise and signal distortion, which is essential for reliable data transmission at high data rates (Wang *et al.*, 2024).

Using the input stage biasing impedance and one of the feedback capacitors, a novel method for constructing a programmable-gain in capacitive feedback TIA that independently adjusts the low- and high-frequency characteristics (Romanova and Barzdenas, 2021). To overcome the Transimpedance limit, there are two methods: Creating a useful tool set for designing high-speed, low-noise TIA for high-sensitivity CMOS optical receivers in both present and future applications (Li *et al.*, 2022). It is proven that the nonlinear decrease in noise indicates that the gain becomes nonlinear in the TIAs (Hameed, 2018). A 10 GHz bandwidth with 43.92 dBΩ TIA gain was achieved using a current-mirror based transimpedance amplifier with inductor feedback simulation (Alsheikhjader, 2020). Using common gate (CG) topology and common source (CS) of transimpedance amplifier (TIA) resulted in low power consumption (Al-Kawaz and Alsheikhjader, 2020; Al-Berwari and Alsheikhjader, 2022). The extremely low level of power consumption is measured by using the common-source common-gate input stage with active inductor feedback (Othman and Alsheikhjader, 2023). Transimpedance amplifiers are essential to offer low power consumption, high gain, and wide bandwidth (Kosykh *et al.*, 2018). Under a 1.5V supply voltage, a TIA gain of 59.885 dBΩ, a bandwidth of 6.9 GHz, and an input-referred noise of $7.925pA/\sqrt{H_z}$, and a minimum power of 872.965 μW was achieved (Elbadry *et al.*, 2020). As a result of reduced input impedance, this configuration will increase gain, and high the bandwidth, and reduce output impedance, providing better results of transimpedance gain (Abu-Taha and Yazgi, 2016). In 130 nm CMOS technology, a common source (CS) amplifier with active inductive peaking was used to achieve a 2.5 Gbit/s TIA (Atef and Abd-earthman, 2014).

This work aims to achieve low levels of power consumption and input referred noise current spectral density due to their high demands in industrial applications.

MATERIALS AND METHODS

Proposed TIA topology:

The proposed TIA topology is illustrated in Fig. (1) as follows:

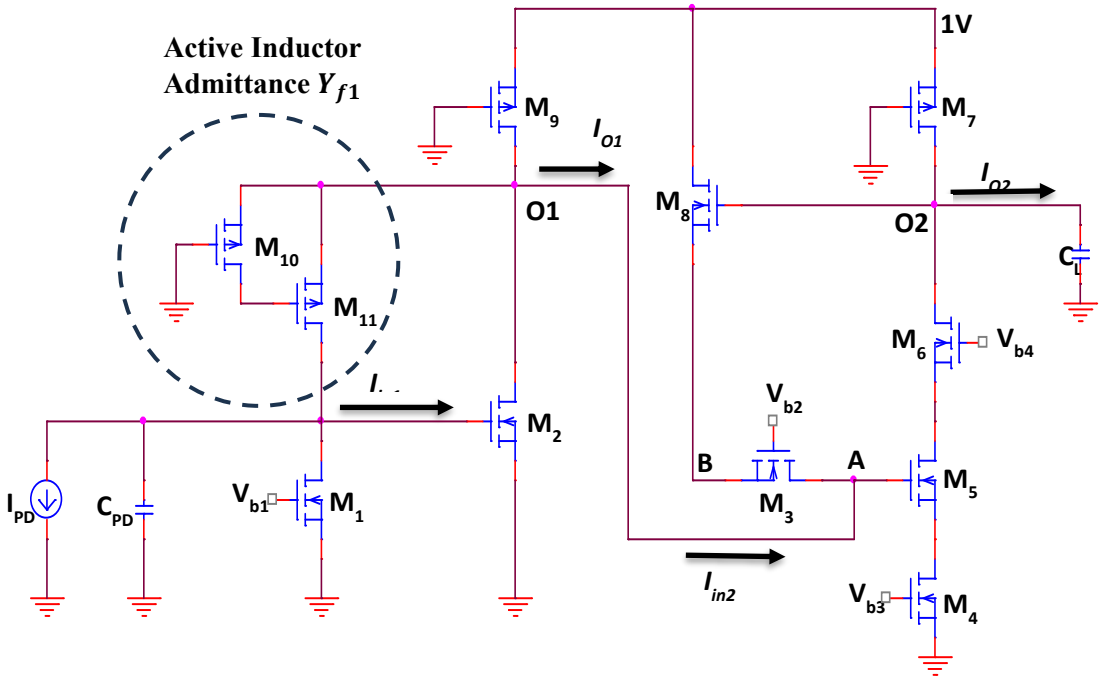

Fig. 1: Proposed TIA topology.

The above topology consists of an input stage of the CS core of amplifying transistor M_2 with active local feedback of two PMOS transistors M_{10} and M_{11} structures with a collective admittance of Y_{f1}. The Norton-based photodiode current I_{PD} is in parallel with dominant photodiode parasitic capacitor C_{PD}. The degenerated output resistance of transistor M_1 provides a parallel configuration with C_{PD} in which their equivalent resistance enables drain current passage to ground.

The output current I_{O1} of the input stage can lead to actual current gain (I_{O1}/I_{PD}) and that is the purpose of having an input stage that works in conjunction with the subsequent second stage which consists of a CS input terminal at the gate of transistor M_5 and a source follower output terminal of transistor M_8. The current I_{in2} entrance of this stage is at node A where a voltage drop occurs effectively at the gate of transistor M_5 leading to drain current conduction and hence enabling the source of the biasing transistor M_6 and eventually more voltage swing at the output node O_2.

Input stage analysis and derivation

Given the fact that the frequency-dependent active inductor feedback impedance is given below and that is based on the general formula (Razavi, 2012):

$$Z_{f1} = \frac{r_{O10}C_{gs11}S + 1}{g_{m11} + C_{gs11}S} \quad \ldots\ldots\ldots (1)$$

The DC active inductor feedback resistance $(S = 0)$ becomes $(R_{f1} = 1/g_{m11})$, so that the loading of R_{f1} on the PMOS current source resistor r_{O9} cannot be neglected given their parallel configuration as given in the input stage circuit model of Fig. (2). The active inductor feedback admittance Y_{f1} denoted in Fig. (1) can be expressed as the inversion of Equ. (1).

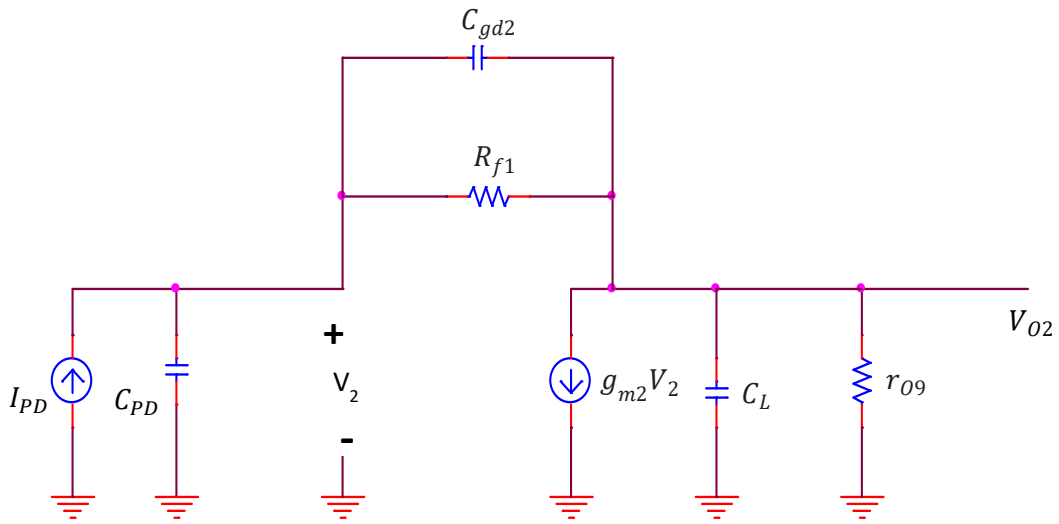

Fig. 2: The input stage DC model.

Evidently and from the above small signal model,

$$V_2 = I_{PD}R_{f1} + V_{O1} \quad \ldots\ldots\ldots (2)$$

In which can be defined as:

$$I_{PD} = g_{m2}\left(I_{PD}R_{f1} + V_{O1}\right) + \frac{V_{O1}}{r_{O9}} \quad \ldots\ldots\ldots (3)$$

It is therefore, the DC transimpedance gain of the input stage is described as follows:

$$Z_{TIA1,DC} = \frac{V_{O1}}{I_{PD}} = -\frac{g_{m2}R_{f1} - 1}{g_{m2}r_{O9} + 1}r_{O9} \quad \ldots\ldots\ldots (4)$$

The DC output resistance of transistor M_2 is parallel with r_{O9}. Theoretically, if $g_{m2}R_{f1} \gg 1$ and $g_{m2}r_{O9} \gg 1$, then, $Z_{TIA1} \approx -R_{f1}$. So far as the input resistance is concerned.

$$R_{in1} = \frac{R_{f1} + r_{O9}}{g_{m2}r_{O9} + 1} \quad \ldots\ldots\ldots (5)$$

In which the output resistance of the input stage is expressed as:

$$R_{O1} = r_{O9} \| \frac{1}{g_{m2}} \quad \ldots\ldots\ldots (6)$$

The f_{-3dB} bandwidth can be expressed in terms of input resistance R_{in1} and total input capacitance $C_{in,tot}$ as follows:

$$f_{-3dB} = \frac{1}{2\pi}\frac{1}{R_{in1}C_{in,tot}} \quad \ldots\ldots\ldots (7)$$

Where $C_{in,tot} = C_{PD} + C_{db1} + C_{db11} + C_{gs2}$, the small signal high frequency model of the input stage is drawn as:

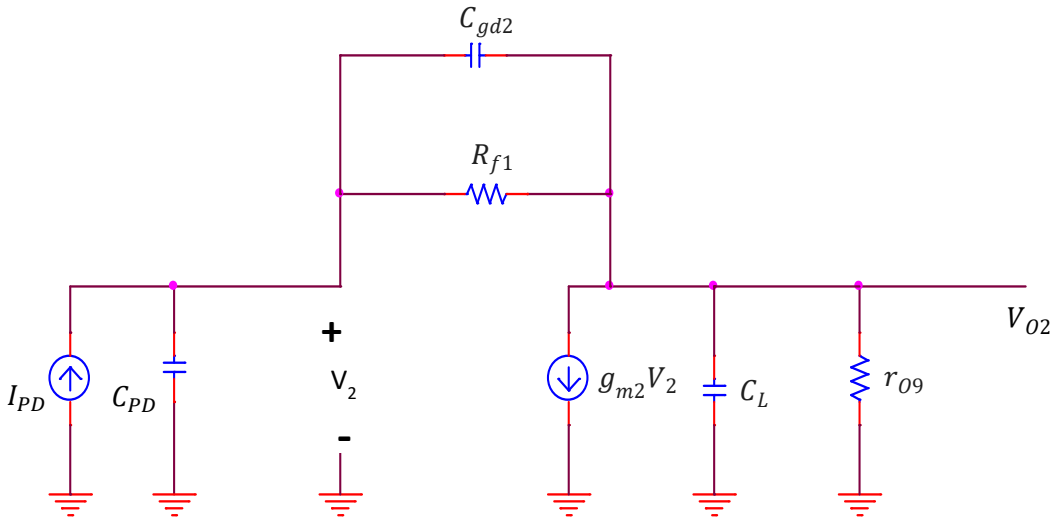

Fig. 3: High-frequency small-signal model of the input stage.

The frequency-dependent TIA1 gain of the input stage is expressed as:

$$Z_{TIA1}(S) = \frac{V_{O1}}{I_{PD}} = \frac{(R_{f1}C_{gd2}S + 1 - g_{m2}R_{f1})r_{O9}}{R_{f1}r_{O9}\zeta S^2 + [R_{f1}(1 + g_{m2}r_{O9})C_{gd2} + r_{O9}C_L + (R_{f1} + r_{O9})C_{in,tot}]S + 1 + g_{m2}r_{O9}} \quad (8)$$

Where $\zeta = C_F C_L + C_L C_{in,tot} + C_{in,tot} C_F$, and if $(S = 0)$, then the above equation is reduced to DC TIA gain of Equ. (4). The frequency-dependent output impedance is represented as:

$$Z_{O1}(S) = r_{O9} \left\| \frac{1}{SC_L} \right\| \frac{1}{g_{m2}} \quad \ldots\ldots\ldots (9)$$

Second stage analysis and derivation

As for the TIA second stage, following the current convention of I_{in2}, the TIA gain Z_{TIA2} is therefore given as:

$$Z_{TIA2} = \frac{V_{O2}}{I_{in2}} = \frac{s^2 a + sb + c}{s^4 A + s^3 B + s^2 C + D} \quad \ldots\ldots (10)$$

Where:

$$a = r_{f3}\left(C_{gs8} r_{ds7} C_{gs5} + C_{gs8} C_{gs5} r_{f3}\right)$$
$$b = \left(C_{gs8} r_{ds7} + r_{f3}\left(g_{m8} C_{gs5} r_{f3} + C_{gs8} + C_{gs5}\right)\right)$$
$$c = -g_{m5} g_{m8} r_{f3}$$
$$A = \left(C_{gs8}\right)^2 r_{ds7} \left(C_{gs5}\right)^2 \left(r_{f3}\right)^2$$
$$B = C_{gs8} r_{ds7} C_{gs5} r_{f3}\left(C_{gs5} r_{f3} g_{m8} + C_{gs8}\right)$$
$$C = C_{gs8}(r_{ds7} g_{m8} - g_{m5} - 1) - C_{gs5}\left(g_{m5} g_{m8} - g_{m8} r_{f3} - 1\right)$$
$$D = -g_{m8}\left(g_{m5} + r_{f3}\right)$$

As a result, the overall TIA gain is introduced as $I_{O1} = I_{in2}$:

$$Z_{TIA} = \frac{I_{O1}}{I_{PD}} \times \frac{V_{O2}}{I_{in2}}$$

Noise analysis

Following on the noise equivalent circuit in Fig. (3), the drain current of transistor M_2 equals to $g_{m2}\left(V_{n,O1} - V_{n,R_{f1}}\right)$, as a result of the current summation at the output node O_1, the noise voltage at this node becomes.

$$V_{n,O1} = \frac{-I_{n,M2} + I_{n,r_{O9}} + g_{m2}V_{n,R_{f1}}}{g_{m2}r_{O9} + 1} r_{O9} \quad \ldots\ldots\ldots (11)$$

The input referred noise current (mean square) is obtained when dividing both sides of the above equation by the Z_{TIA1} gain assuming $g_{m2}r_{O9} \gg 1$ as follows:

$$\overline{I_{n,in}^2} = \frac{\overline{I_{n,M1}^2} + \overline{I_{n,r_{O9}}^2} + g_{m2}^2\overline{V_{n,R_{f1}}^2}}{g_{m2}^2 R_{f1}^2} = \frac{4kT\gamma}{g_{m2}R_{f1}^2} + \frac{4kT}{g_{m2}^2 R_{f1}^2 r_{O9}} + \frac{4kT}{R_{f1}} \quad \ldots\ldots\ldots (12)$$

RESULTS

The TIA gain shown in Fig. (4) indicated 56.8 dBΩ at the point of bandwidth of 1 GHz. Despite the limitation imposed by the input stage common source configuration, the extent of the bandwidth involved was enhanced by the active inductor feedback installment. A frequency response of this type is suitable for Gb/s application.

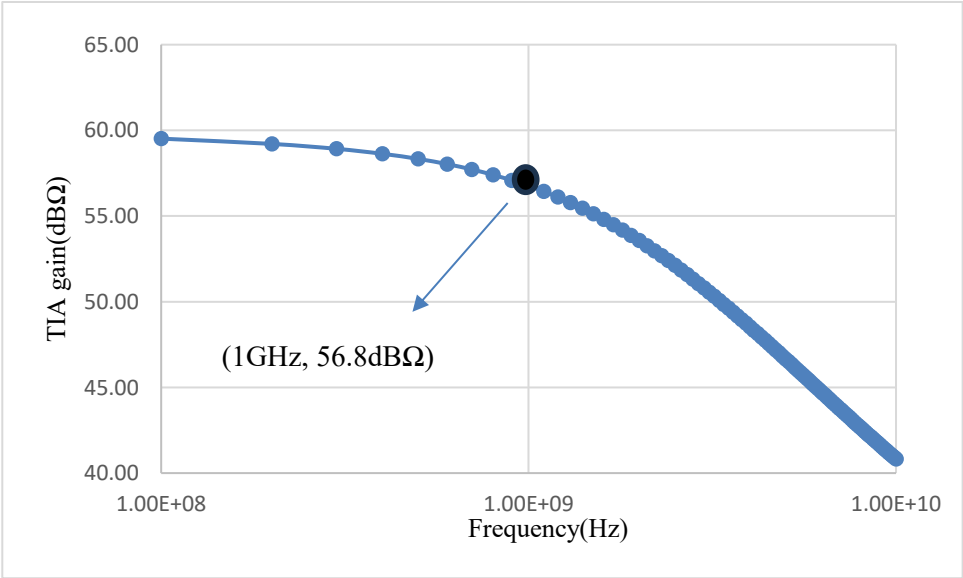

Fig. (4): Overall TIA gain for the proposed design.

In Fig. (5), the frequency response of the input impedance is illustrated in which a 1.58 MΩ is exhibited at 1 GHz bandwidth. A noticeable reduction in impedance is shown as the signal frequency is increased. A gap of 14 MΩ is reduced between 100 MHz up to 1 GHz signal frequency.

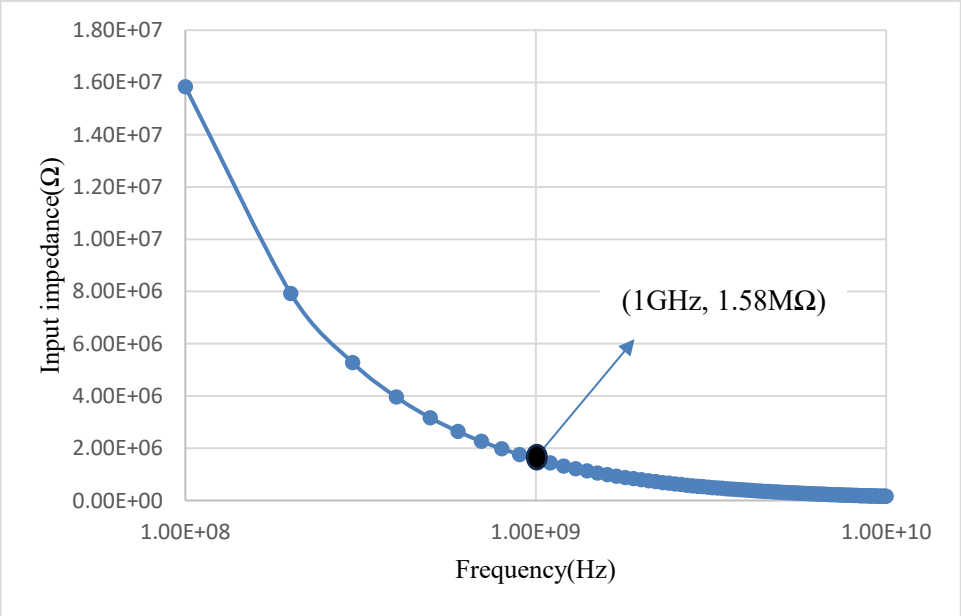

Fig. (5): Frequency response of the input impedance.

Regarding Fig. (6), the input referred noise current spectral density appears to have 15.3 $pA/\sqrt{H_z}$ at the 1 GHz bandwidth. This low magnitude of noise can have real impact on the TIA performance as the lowering magnitude mechanism is explained in section 6.

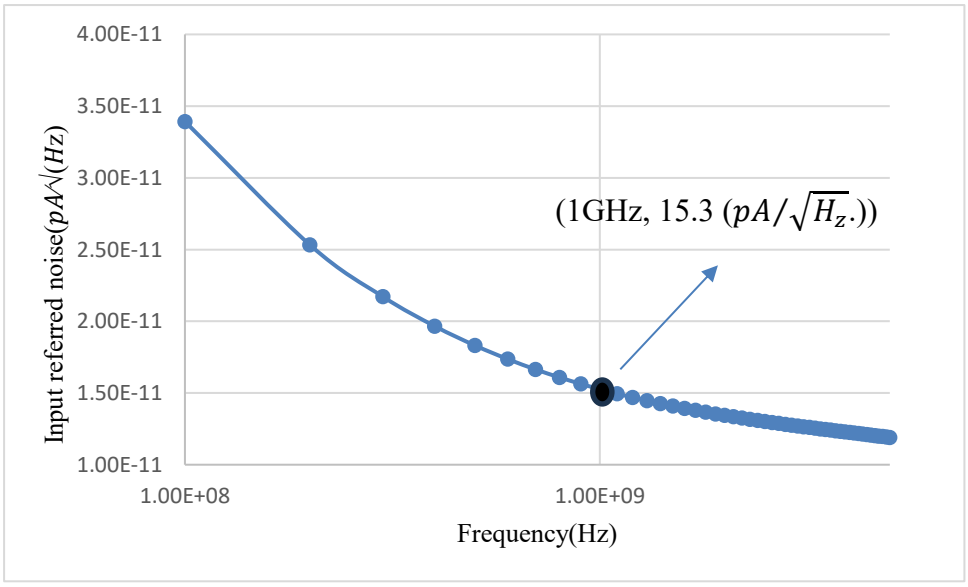

Fig. (6): Input-referred noise current spectral density for the proposed topology.

The lowest total power consumption is reported in this work for the proposed TIA topology. A 0.41 mW is registered which is an average power consumption, while each transistor consumption is shown in Fig. (7). Transistor M_7 showed the highest consumption in the circuit, while transistors M_1-M_4 showed near zero levels for that matter.

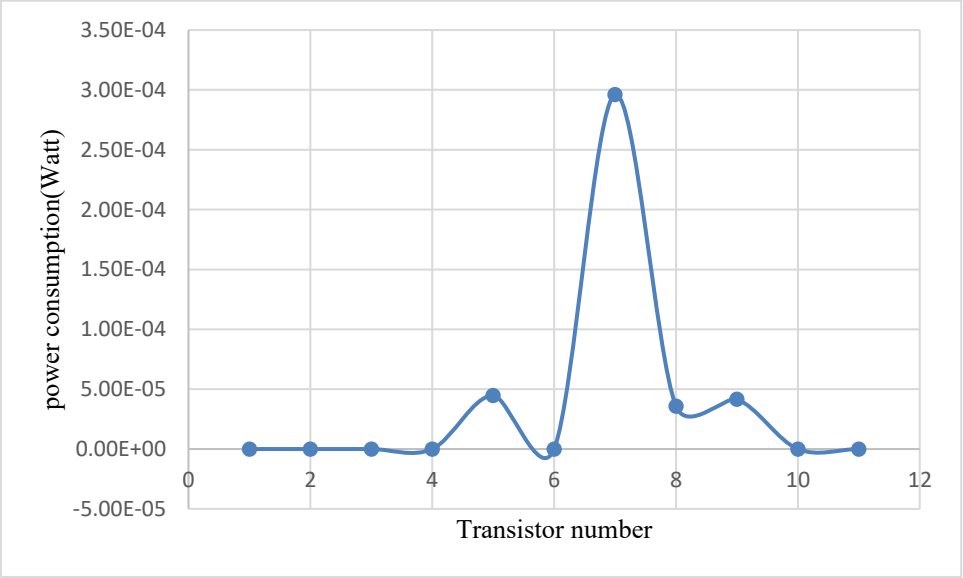

Fig. (7): Power consumption as per each transistor number.

Comparative performance analysis

As in (Table 1), having achieved a 56.8 dBΩ of TIA gain in this work, it is far larger than 7.6 dBΩ shown in literature (Kim and Buckwalter, 2012). However, there is a considerable difference in bandwidth, and that will be application-specific matter. Having said that, the level of power consumption and input referred noise current is far lower in this work than previous literature (Kim and Buckwalter, 2012). So far as TIA gain magnitude of previous literature (Xie *et al.*, 2018), it is higher than the reported data in this work, however, in the mentioned literature, it lags in terms of power consumption and input referred noise current reported in this article. Finally, the 10 MHz bandwidth reported in previous literature (Muthukumaran and Ramachandran, 2022) makes it less attractive in terms of fiber optic application despite its low levels of power consumption and input referred noise current.

Table 1: Comparative performance analysis.

Ref.	(Kim and Buckwalter, 2012)	(Xie *et al.*, 2018)	(Muthukumaran and Ramachandran, 2022)	This Work
Year	2012	2018	2022	2025
CMOS Technology	45 nm	45 nm	45 nm	45 nm
TIA Gain (dBΩ)	7.6	74.4	140	56.8
Bandwidth (GHz)	33	23	10 MHz	1
Input Referred Noise ($pA/\sqrt{Hz}$)	20.5	12	4.6	15.3
Power Consumption (mW)	9	36.6	0.01	0.41
dc Supply Voltage (V)	1	1	-	1

DISCUSSION

To start with, the input stage was designed to have a current gain, while the subsequent stage was designed to have a transimpedance gain. Within the input stage, the active inductor feedback impedance was configured to resonate with the input capacitance so that limited inductive peaking occurs with no overshoot concerning the gain frequency response of Fig. (4). At high frequencies, the active inductor feedback impedance Z_{f1} becomes extremely high leading an exceptionally low admittance Y_{f1} and hence very low fractional feedback leading to a limited voltage swing at the drain of transistor M_1. This voltage swing is subtracted (negative feedback) from the signal

emanating from the photodiode therefore, ending up in a net gate-to-source voltage of transistor M_2 enabling it to conduct. In the active inductor setup, capacitor C_{gs11} can work as an open circuit in which transistor M_{11} effectively becomes diode-connected, while at high frequencies however, the gate of transistor M_{11} becomes at ac ground. Furthermore, since there are no possible current transients within the active inductor, hence, there is not much of an energy dissipation at the gate of transistor M_2 leading to less noise contribution. Eventually, to have high active inductor impedance at high frequency, the equivalent inductance L_{eq} can be tuned if $r_{O10} \gg 1/g_{m11}$, then it becomes:

$$L_{eq} = \frac{r_{O10} C_{gs11}}{g_{m11}} \quad \ldots\ldots\ldots (13)$$

The high small signal resistance of PMOS loads of transistors M_7 and M_9 facilitates independent node voltages such as O_1 and O_2 respectively that enables a stable drain current path through them. As a result, a relaxation of a trade-off between voltage gains and voltage headroom is achieved given that the voltage gain of the transistor M_2 (amplifying transistor) is $-g_{m2}R_D$ where R_D in this case is $r_{O9} \| R_{f1} \| (R_{G5} \| r_{db3})$.

So far as the lowest possible input referred noise current spectral density, it is all down to the extremely low active inductor feedback admittance Y_{f1}, in which it corresponds to the inverted feedback impedance R_{f1} represented in three terms on Equ. (12). In this equation, when it is assumed that $g_{m2} r_{O9} \gg 1$, the second terms go to the lowest value contributing even further to the reduction in noise contribution. The power consumption reduction is mainly due to the output resistance r_O of each transistor, given the fact that $r_O = 1/(\lambda I_D)$, hence, the highest output resistance means the lowest possible drain current I_D where is the channel length modulation coefficient. Low drain current leads to low power consumption as per each transistor given that the power consumption equals to $I_D V_{DD}$ where V_{DD} is the budget supply voltage for the entire circuit.

CONCLUSIONS

The obtained results by using a common-source input stage-based transimpedance amplifier are low power consumption (0.41 mW) and input-referred noise current (15.3 $pA/\sqrt{H_z}$) with high TIA gain and moderate f_{-3dB} bandwidth. These results support the main goal of the research, which is to obtain the lowest energy consumption and the maximum gain value for the transimpedance. Relying on the mathematical derivation and simulation of the transimpedance for a high range of frequencies is of great importance in obtaining these results. This method provides a typical framework that can be used to reduce costs by adopting an optimal transimpedance. The real difficulty in obtaining an ideal interface impedance was the process of finding a design that simulated the input signal. Future researchers can expand the scope of this research and study the impact of fiber optic circuit applications. In addition, the results obtained from this work can be used in industrial applications by reducing TIA power consumption.

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مضخم الممانعة البينية القائم على مرحلة إدخال المصدر المشترك لأنظمة الألياف الضوئية

مهند مؤيد الياس **محمد صبحي الشيخ جادر**

قسم الفيزياء/ كلية العلوم/ جامعة الموصل/ موصل/ العراق

الملخص

يُقترح في هذا العمل مكبر الممانعة البينية (TIA) مع تحليلاته الرياضية. أثبتت مرحلة إدخال المصدر المشترك (CS) أنها تُظهر استهلاكًا منخفضًا للغاية بالنسبة للقدرة علاوة على انخفاض تيار الضوضاء المشار اليها بالدخل (الكثافة الطيفية) مع كسب TIA مرتفع وعرض نطاق f_{-3dB} معتدل. تم الحصول على نتائج المحاكاة لهذه الدائرة كما يلي: عن قيمة قدرها 56,8 dBΩ في ربح TIA وعند عرض نطاق قدره 1 جيجا هرتز. تم تحقيق استهلاك منخفض للقدرة قدره 0.41 ميجاوات والذي يتوافق مع مقدار تناقص تيار الضوضاء بمقدار $15.3\ pA/\sqrt{H_z}$ ويبدو أن استرخاء المفاضلة قد حدث بين كسب TIA ناحية، وانخفاض مرجعية ضوضاء الدخل من بينما من ناحية أخرى، حدث انخفاض مشترك في استهلاك القدرة وتيار الضوضاء المشار إليه. تمثل النتائج الرئيسية المذكورة أعلاه التحديات الرئيسية في التطبيقات الصناعية وخاصة في تقليل استهلاك قدرة TIA كطلب خاص بالتطبيقات مع إشارات السلامة العالية تتضمن تيار ضوضاء منخفض المدخلات. بالإضافة إلى ذلك، يمكن استخدام النتائج التي تم الحصول عليها من هذا العمل في التطبيقات الصناعية عن طريق تقليل استهلاك الطاقة TIA.

الكلمات الدالة: دائرة مكبر الممانعة البينية، توصيلة النهاية–الأمامية، تركيب المصدر المشترك، المكبر البصري، الممانعة البينية.